INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	~~10882468~~ 10/822,468
	Filing Date	2004-04-12
	First Named Inventor	Mitchell Alsup
	Art Unit	2183
	Examiner Name	George D. Zalepa
	Attorney Docket Number	5500-92000

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W	1	6247121		2001-06-12	Akkary et al	
W	2	3896419		1975-07-22	Lange et al	
W	3	5381533		1995-01-10	Peleg	
W	4	6449714		2002-09-10	Sinharoy	
W	5	6339822		2002-01-15	Miller	
W	6	6256727		2001-07-03	McDonald	
W	7	6185675		2001-02-06	Kranich et al	
W	8	6823428		2004-11-23	Rodriguez et al	

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	9	6167536		2000-12-26	Moann	
W	10	6357016		2002-03-12	Rodgers et al	
W	11	7003629		2006-02-21	Alsup	
W	12	6345295		2002-02-05	Beardsley et al	
W	13	5930497		1999-07-17	Cherian et al	
W	14	6578128		2003-06-10	Arsenault et al	
W	15	6973543		2005-12-06	Hughes	
W	16	6216206		2001-04-10	Peled et al	
W	17	6233678		2001-05-15	Bala	
W	18	5210843		1993-05-11	Ayers	

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Examiner Initial*	Cite No	Publication Number	Kind Code¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040143721		2004-04-22	Pickett et al	
	2	20020144101		2002-10-03	Wang et al	
	3	20030023835		2003-01-30	Kalafatis et al	
	4	20040083352		2004-04-29	Lee	
	5	20040193857		2006-11-16	Miller et al	
	6	20050125632		2005-06-09	Alsup et al	
	7	20020095553		2002-04-18	Mendelson et al	
	8	20050076180		2005-04-07	Smaus et al	
	9	20050125613		2005-06-09	Kim et al	
	10	20040216091		2004-10-28	Groeschel	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	**Application Number** ~~10882468~~ 10/822,468
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W	1	2281101	GB		2003-04-23			☐
W	2	957428	EP		1999-11-17			☐

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W	1	Jacobson, et al., "Instruction Pre-Processing in Trace Processors," IEEE Xplore, January 1999, 6 pages.	☐
W	2	Yuan Chou, et al., "Instruction Path Coprocessors," March 2000, pp. 1-24.	☐
W	3	Sanjay J. Patel, et al., "replay: A Hardware Framework for Dynamic Optimization," IEEE, Vol. 50, No. 6, June 2001, pp. 590-608.	☐
W	4	Patterson, et al., "Computer Architecture A Quantitative Approach," Second Edition, Morgan Kaufmann Publishers, Inc., 1996, pp. 271-278	☐
W	5	Bryan Black, et al., "The Block-Based Trace Cache," IEEE, 1999, pp. 196-207.	☐

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